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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant : Hsueh-Yuan Pao et al. Attorney Docket No. : IL-11028

Serial No. : 10/644,561 Art Unit: 2634

Filed : August 19, 2003 Examiner: E. File

For : Digital Intermediate Frequency QAM Modulator Using Parallel Processing

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Respectfully submitted,

John P. Wooldridge

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Dated: February 13, 2006

PATENT

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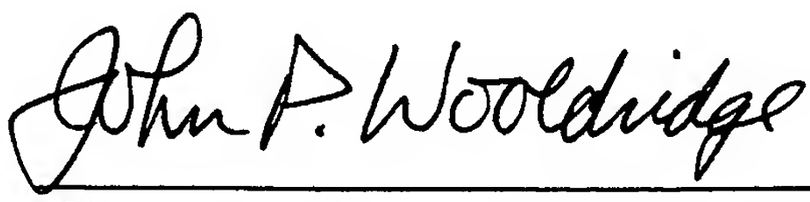

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BRIEF ON APPEAL

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This is an appeal to the Board of Patent Appeals and Interferences from the final rejection of Claims 1-12 mailed September 12, 2005. On December 12, 2005, a timely Notice of Appeal was filed.

I. REAL PARTIES IN INTEREST

The real parties in interest are the Regents of the University of California and the United States of America as represented by the United States Department of Energy.

II. RELATED APPEALS AND INTERFERENCES

Appellant knows of no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-12 are pending on appeal and stand rejected. The rejection of claims 1-12 is appealed. A copy of the claims on appeal is set forth in the Claims Appendix.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent apparatus claims 1, 2, 4 and 6 claim a digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier. Independent method claims 7, 8, 10 and 12 claim a method for processing data with a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier.

As shown in Figure 3 and described in paragraphs 35 and 36 in the published patent application, independent claim 1 provides a serial-to-parallel data converter **300** to convert a string of serial data to a plurality of parallel data; an I and Q mapper **400** to determine the I and Q locations of the data; a plurality of look-up-tables (LUTs) **800** to **803** and **820** to **823** operatively connected to receive and store the I and Q locations; a plurality of adders **113** to **116** to add the storred I and Q locations; a plurality of registers **124** to **127** to collect and store the output data; and a digital to analog converter **200** to convert the output data to analog data. Claim 7 embodies the method of operation of the apparatus of claim 1, and it is also described in paragraphs 35 and 36 with reference to Figure 3.

Independent claim 2 includes the elements of claim 1 and additionally includes multiplexers to collect odd and even subscript output data from the registers, as shown in figures 3, 5 and 6A-6E and described in paragraphs 35, 36 and 51. Claim 7 embodies the method of operation of the apparatus of claim 2,

and it is also described in paragraphs 35, 36 and 51 with reference to figures 3, 5 and 6A-6E.

Independent claim 4 includes all of the elements of independent claim 2 without specifically reciting the serial-to-parallel data converter or the I and Q mapper. Claim 10 embodies the method of operation of the apparatus of claim 4 See paragraph 35, 36 and 51 and figures 3, 5 and 6A-6E.

Independent claim 6 includes all of the elements of independent claim 1 without specifically reciting the serial-to-parallel data converter or the I and Q mapper. Claim 12 embodies the method of operation of the apparatus of claim 6 See paragraph 35, 36 and 51 and figures 3, 5 and 6A-6E.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPPEAL

Whether claims 1-12 are unpatentable over Zhang in View of Becker.

VII. ARGUMENT

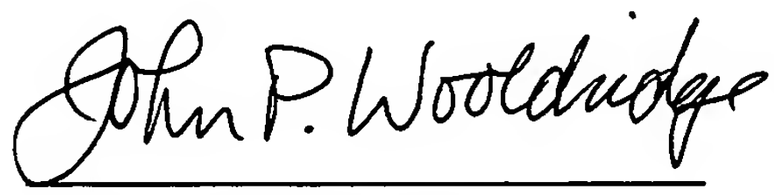
Are claims 1-12 unpatentable over Zhang in View of Becker?

The Examiner admits that Zhang fails to disclose a quadrature amplitude modulator that does not include a multiplier. All of the independent claims in the present application under appeal specifically exclude the use of a multiplier. The Examiner relies upon the secondary reference, Becker, to exclude the use of the multiplier; however, it is not necessary to address the Examiner's argument because the applicants' priority date (August 19, 2002) precedes that of Becker (November 8, 2002).

U.S. Provisional Patent Application 60/404,596, filed August 19, 2002, from which the present application claims priority, describes all aspects of the claimed invention. For example, the exclusion of multipliers is discussed in the provisional application, inter alia, on pages 7 and 17.

Accordingly it is submitted that the rejections of claims 1-12 are improper and should be reversed.

Respectfully submitted,



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VIII. CLAIMS APPENDIX

1. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

2. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are

added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

3. The digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier of claim 2, wherein said at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers, where n is an integer, and wherein said at least one multiplexer is operatively connected to collect from said plurality of registers the subscript

output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

4. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN};

a first multiplexer operatively connected to collect from said plurality of registers only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

a second multiplexer operatively connected to collect from said plurality of registers only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

5. The digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier of claim 4, wherein said first multiplexer comprises nx2 multiplexers, where n is an integer, and wherein said second multiplexer comprises nx2 multiplexers.

6. A digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of

adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

7. A method for processing data with a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and converting a string of serial data into a plurality of parallel data;

determining the I and Q locations of said plurality of parallel data;

storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs, wherein ~~said~~ a plurality of adders are configured A_1 to A_{AN},

wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing said output data comprising IQ_1 to IQ_{IQN} in a plurality of registers; and

converting said output data comprising IQ_1 to IQ_{IQN} to analog data in a digital to analog converter, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

8. A method for processing data in a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and converting a string of serial data to a plurality of parallel data;

receiving said plurality of parallel data in an I and Q mapper and determine the I and Q locations of said plurality of parallel data;

receiving and storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs in a plurality of adders, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting, in a first multiplexer, from said plurality of registers, the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting, in a second multiplexer, from said plurality of registers, the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting, a digital to analog converter, said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

9. The method of claim 8, wherein said first multiplexer comprises nx2 multiplexers, where n is an integer, and wherein said second multiplexer omprises nx2 multiplexers.

10. A method for processing data in a digital intermediate frequency QAM modulator using parallel processing without the use of a multiplier, comprising:

receiving and storing in a plurality of look-up-tables (LUTs), I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting in a first multiplexer only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting in a second multiplexer only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said odd subscript data and said even subscript data to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.

11. The method of claim 10, wherein said first multiplexer comprises nx2 multiplexers, where n is an integer, and wherein said second multiplexer comprises nx2 multiplexers.

12. A method for processing data with a digital intermediate frequency Quadrature Amplitude Modulation modulator using parallel processing without the use of a multiplier, comprising:

receiving and storing, in a plurality of look-up-tables (LUTs) I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said output data comprising IQ_1 to IQ_{IQN} to analog data, wherein said Quadrature Amplitude Modulation modulator does not include a multiplier.